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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,413	12/08/2003	Xiang Liu	Liu 25-18-17-7	2453

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EXAMINER	
PASCAL, LESLIE C	

ART UNIT	PAPER NUMBER
2613	

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10/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,413	LIU ET AL.	
	Examiner	Art Unit	
	Leslie Pascal	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. This is in response to the applicants' arguments with regard to the pre-appeal brief request of 7-24-08. It would appear that the examiner could have gone to the Board of Appeals, because the arguments presented had never been made before the final office action. Further, the applicants' specification teaches that the integration is well known with regard to sampling windows (page 5, lines 17-19). This section of the applicants' specification teaches that the typical prior art has a sampling width and this affects the integration (which would make this feature either obvious or inherent). The examiner has chosen to provide another office action in order to add the 101 rejection of paragraph 3 and to make the 103 rejection stronger before going to the Board of Appeals.

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-10 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated

by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 3-11, 13-21 and 23-24 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3-4, 6-7, 11, 13-14,21 and 23 of copending Application No. 10/782231. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending application has more elements than the present application, the present application claim 1 reads on claims 1 and 3 of the copending application. Claim 1, lines 1-3 read on claim 1, lines 1-3 of the related application. Claim 1, lines 4-5 read on claim 1, lines 4-5 of the related application. Claim 1, lines 6-9 read on claim 3, lines 3-5 of the related application. Claim 1, lines 10-13 read on claim 1, lines 7-10 of the related application. Claim 1, lines 14-16 read on claim 3, lines 8-9 of the related application except that the related application does not claim specifics of the window width which was amended. He claims that he has two windows within a one bit length, it would appear obvious, if not inherent that the window is less than a bit length since there are two "windows" within the bit period. He also claims that the window is selected to reduce contribution (as the present application does). It would appear that

the window must be selected to be less than the bit length in order to provide this reduction (if one invention has the window less than the bit length and it provides the reduction, it would appear inherent that the other application must also have a window less in order to provide the reduction). Further, when using the disclosure as a dictionary for the window, it is clear that the window width is less than a bit slot. Claim 24 relates to the method of claim 1. In regard to claims 4, 14 and 23, see claim 6 of the copending application. In regard to claims 5 and 15, see claim 7 of the copending application. In regard to claim 11, see claims 3-4 and 11 of the copending application and the obvious statement for claim 1 above. In regard to claim 21, see claims 1, 3-4 and 20 of the copending application and the obvious statement for claim 1 above. In regard to claims 3 and 13, in that the sampling window would be a function of the eye opening in order to provide the highest quality signal, it would have been obvious to use the eye diagram in order to select a sampling window width. In regard to claims 6 and 16, in that the sampling window would be a function of the clock signal in order to provide the highest quality signal, it would have been obvious to align the sampling window with the clock in order to provide a proper sampling of the signal. In regard to claims 7, 10, 17 and 20, in that the sampling window would be a function of the duty cycle and in order to provide the highest quality signal, it would have been obvious to use the duty cycle in order to select a sampling window width. In regard to claims 8-9 and 18-19, the applicant teaches that it is not critical what percentage the sampling width is with respect to the bit length. It would have been obvious to use plural small (small percentage which would be less than 20%) sampling widths in order to provide a

proper sampling of the signal. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 5-13, 15-22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller (2003/0170022) in view of disclosure of typical prior art in applicants' specification.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing

that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claims 1, 11, 21 and 24, Moeller discloses: converting an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal (e.g., 230 in Fig. 2, 530 in Fig. 5); sampling the electrical signal using at least one sampling windows contained within a time interval having a one-bit length (the multiple sampling points in Fig. 4 correspond to one bit slot) to generate bit estimate values (multiple Sampling points in Fig. 4), and comparing the first result with a first decision threshold value to generate a first bit estimate value (e.g., threshold in Fig. 4); and comparing the second result with a second decision threshold value to generate a second bit estimate value (e.g., threshold in Fig. 4); and applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5).

Although Moeller does not specifically teach integration in order to provide the first and second results, see page 5, lines 17-19 of the applicants' specification which teaches that it is well known in a prior art system to use a sampling window less than the bit length and integrating it in order to provide the result signal. Therefore, it would have been obvious to integrate over the sampling window of Moeller as taught by the applicants' specification that a typical prior art configuration integrates over the sampling window in order to produce a result signal. Each sampling window has a width (each sampling point in Fig. 4 of Moeller has its own finite width); the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each

waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "x" (waveforms below the threshold represent "0", waveforms above the threshold represent 'T'); and for each sampling window:
a waveform is integrated over the sampling window width to generate a corresponding bit estimate value (integration is implied in the decision circuit 240 to generate the output bit estimate values); and Moeller does not expressly disclose:
the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms.
However, such a selection of sampling window width is intuitively obvious. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to provide such a selection of sampling window width. One of ordinary skill in the art would have been motivated to do this in view of an obviously undesirable counterexample. That is, consider the option of a sampling window that is as wide as the bit slot. With such a wide sampling window, the "1" waveforms of pulses with timing jitter from adjacent bit slots can adversely contribute to the integration results corresponding to "0" waveforms. This contribution can lead to inaccurate sampling results. Accordingly, it follows that one would be motivated to select a sampling window width to reduce this contribution, e.g., a sampling window width that is narrower than the bit slot. (The applicants' specification further teaches that the sampling window in a typical prior art configuration which ha a relatively large width is 30% of the bit length on page 5, lines 17-18). For example, lower threshold values may help avoid spontaneous beat noise at the mark level of a sampling window, and higher threshold values may help avoid

spontaneous beat noise and thermal noise at the space level of a sampling window. Regarding claims 5 and 15, Moeller discloses: The method of claim 1, comprising: generating a first clock signal based on the electrical signal (10 GHz clock tone in paragraph [0021]); multiplying a frequency of the first clock signal to generate a second clock signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]); and sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]). Regarding claim 14, Moeller discloses: The receiver of claim 11, comprising: a decision circuit (e.g., decision circuit 240 in Fig. 2) coupled to the signal converter; a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal (implied circuitry for recovering the 10 GHz clock tone in paragraph [0021]); and a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal (4o GHz clock from 1:4 frequency multiplier in paragraph [oo21]), wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]. regard to claims 3 and 13, in that the sampling window would be a function of the eye opening in order to provide the highest quality signal, it would have been obvious to use the eye diagram in order to select a sampling window width. In regard to claims 6 and 16, in that the sampling window would be a function of the clock signal in

order to provide the highest quality signal, it would have been obvious to align the sampling window with the clock in order to provide a proper sampling of the signal. In regard to claims 7, 10, 17 and 20, in that the sampling window would be a function of the duty cycle and in order to provide the highest quality signal, it would have been obvious to use the duty cycle in order to select a sampling window width. In regard to claims 8-9 and 18-19, the applicant teaches that it is not critical what percentage the sampling width is with respect to the bit length. It would have been obvious to use plural small (small percentage which would be less than 20%) sampling widths in order to provide a proper sampling of the signal. In regard to claims 2, 12 and 22, see paragraph 29 of the reference which teaches that he adjusts the threshold in order to adjust the "1"s and "0"s, it would have been obvious to adjust the threshold in reduce noise since he teaches adjusting the threshold to improve the levels.

8. Claims 4, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller as applied to the claims above, and further in view of Yonenaga et al. (Ref BF on the IDS of 5-16-05, "Dispersion-tolerant optical transmission system using duo binary transmitter and binary receiver", hereinafter 'Yonenaga").

Regarding claims 4, 14 and 23, Moeller does not expressly disclose the method of claim 1, wherein the optical signal is an optical duo binary signal. Although Moeller considers return-to-zero (RZ) coding (paragraph [0017]), notice the duo binary coding of Yonenaga (p. 1530, col. 2, middle paragraph - p. 1531, 1st paragraph). At the time the invention was made, it would have been obvious to one of ordinary Skill in the art to employ the duo binary coding of Yonenaga. One of ordinary skill in the art would have been motivated to do this for any of the following advantages: higher tolerance to fiber chromatic dispersion that limits transmission distance and suppression of stimulated Brillouin scattering (SBS) (Yonenaga, p. 1530-1531, bridging paragraph). Moeller in view of Yonenaga discloses the receiver wherein the optical signal is an optical duo binary signal (Yonenaga, p. 1530, col. 2, middle paragraph - p. 1531, 1st paragraph).

9. In regard to the applicants' arguments that the double patenting should be withdrawn in this case, in view of the 103 rejections, this argument is moot. If there are no art rejections, the double patenting rejection will be withdrawn.

With regard to the applicants arguments with regard to the integration, see the changes to the rejection. In view of the applicants' specification which teaches that the "typical prior art" integrates over a sampling window less than one bit, it is clear that such a feature is obvious. In regard to the argument that Moeller has a sampling point which is not a window width, see the abstract, paragraph 8-paragraph 9 of Moeller. He teaches sampling more than once within the bit period. Paragraph 7 teaches that the sampling in conventional systems is done at a point in the bit period, but Moeller teaches that there are benefits to sampling more than once in the bit period and using some form of logic to determine the state of the signal. The applicant teaches that a typical prior art uses integration to determine the state. Therefore, it would have been obvious to use integration in order to determine the logic state of Moeller (022). Throughout the document, Moeller teaches sampling over a window. In regard to the applicants' arguments that the examiner has not provided enough evidence that it is well known to use a sampling window and integration, the applicants' specification teaches that it is well known in the "typical prior art".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie Pascal whose telephone number is 571-272-3032. The examiner can normally be reached on Monday- Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leslie Pascal/
Primary Examiner
Art Unit 2613